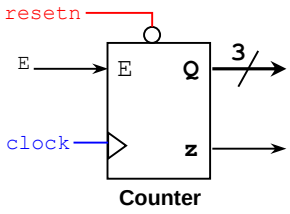
Homework 4

(Due date: March 31st @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

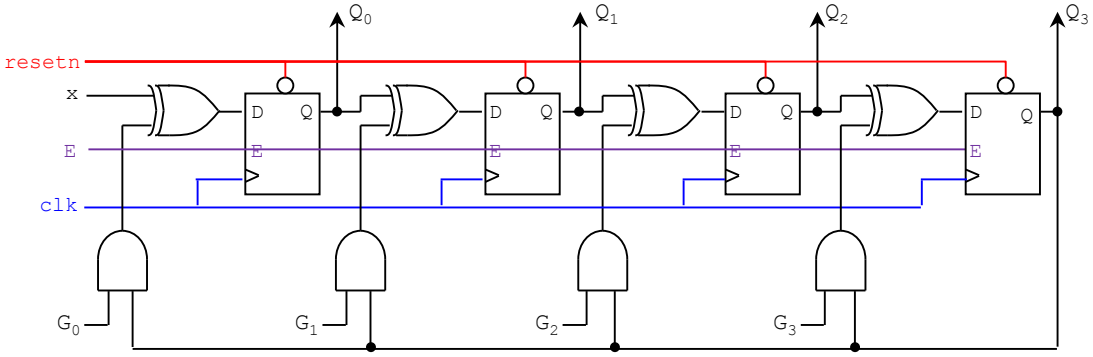


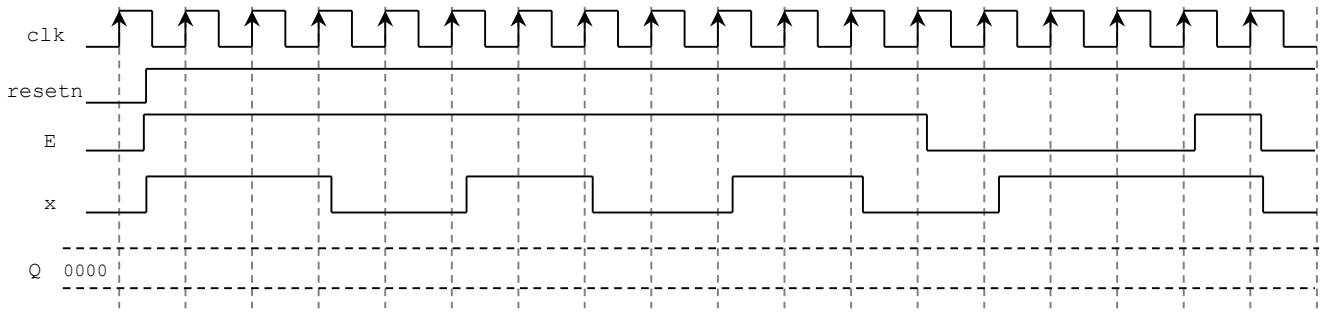
- Design a counter using a Finite State Machine (FSM):
  Counter features:
  - ✓ Count: **000**, 010, 111, 011, 110, 100, 001, 101, **000**, 010, 111, …
  - ✓ $resetn$: Asynchronous active-low input signal. It initializes the count to "000"
  - ✓ Input E: Synchronous input that increases the count when it is set to '1'.
  - ✓ output z: It becomes '1' when the count is 101.

- Provide the State Diagram (any representation), State Table, and the Excitation Table. Is this a Mealy or a Moore machine? Why? (10 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (5 pts)

PROBLEM 2 (15 PTS)

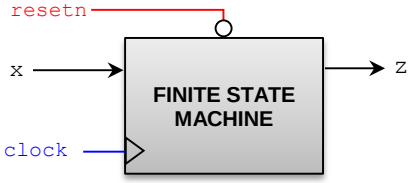
- Complete the timing diagram of the following circuit. $G = G_3G_1G_2G_0 = 1001$, $Q = Q_3Q_2Q_1Q_0$



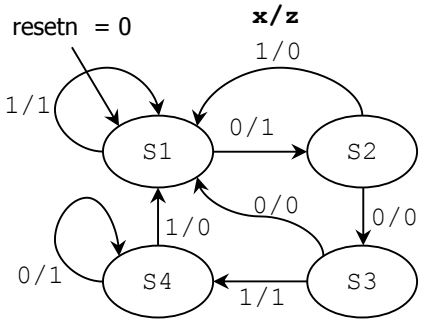


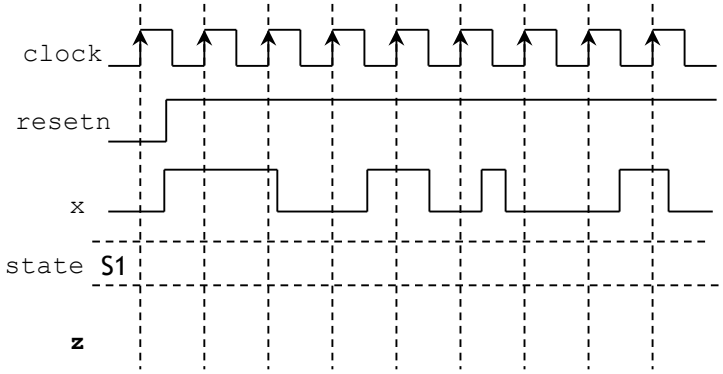
PROBLEM 3 (30 PTS)

- Sequence detector (with overlap): (10 pts)
  Draw the state diagram (any representation) of a circuit (with an input x) that detects the following sequence: 1010011. The detector must assert an output z when the sequence is detected.



- Complete the timing diagram of the following FSM. Is this a Mealy or a Moore machine? Why? (5 pts)

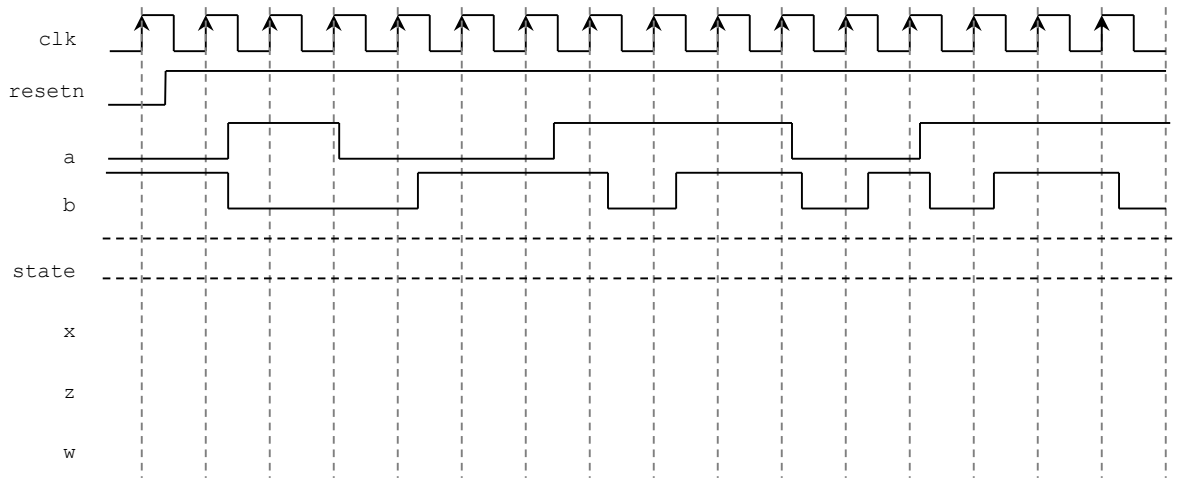




- Provide the state diagram (in ASM form) and complete the timing diagram of the FSM whose VHDL description is listed below. (15 pts)

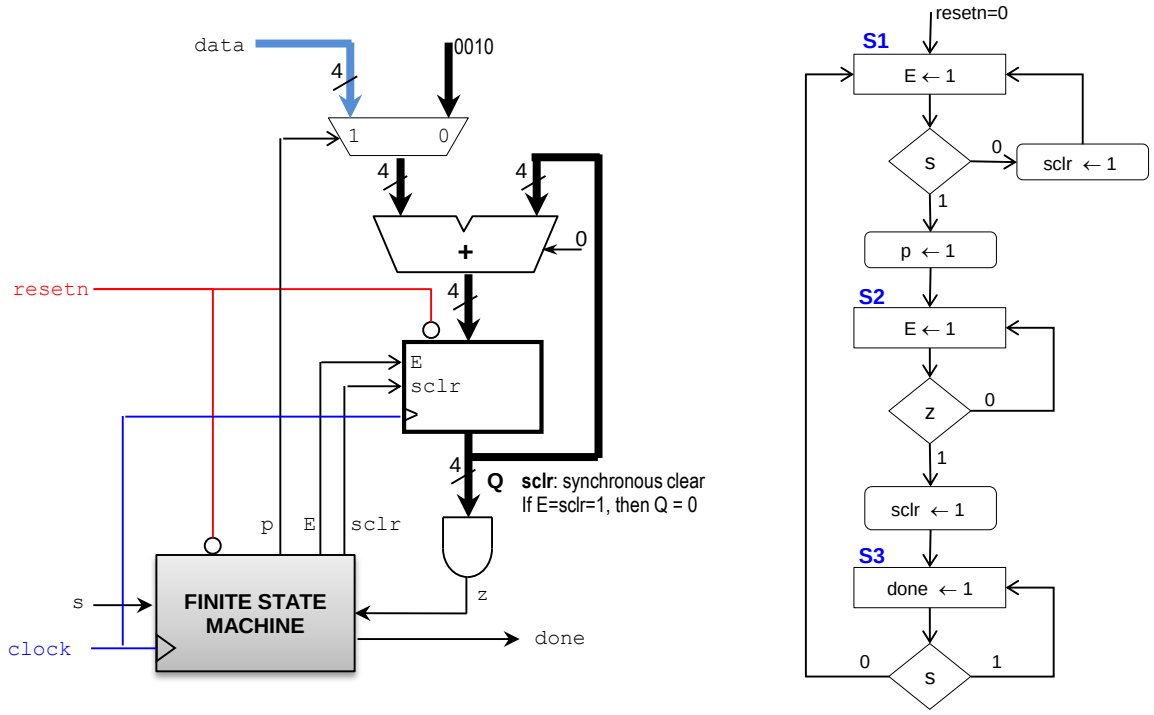
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end circ;
```

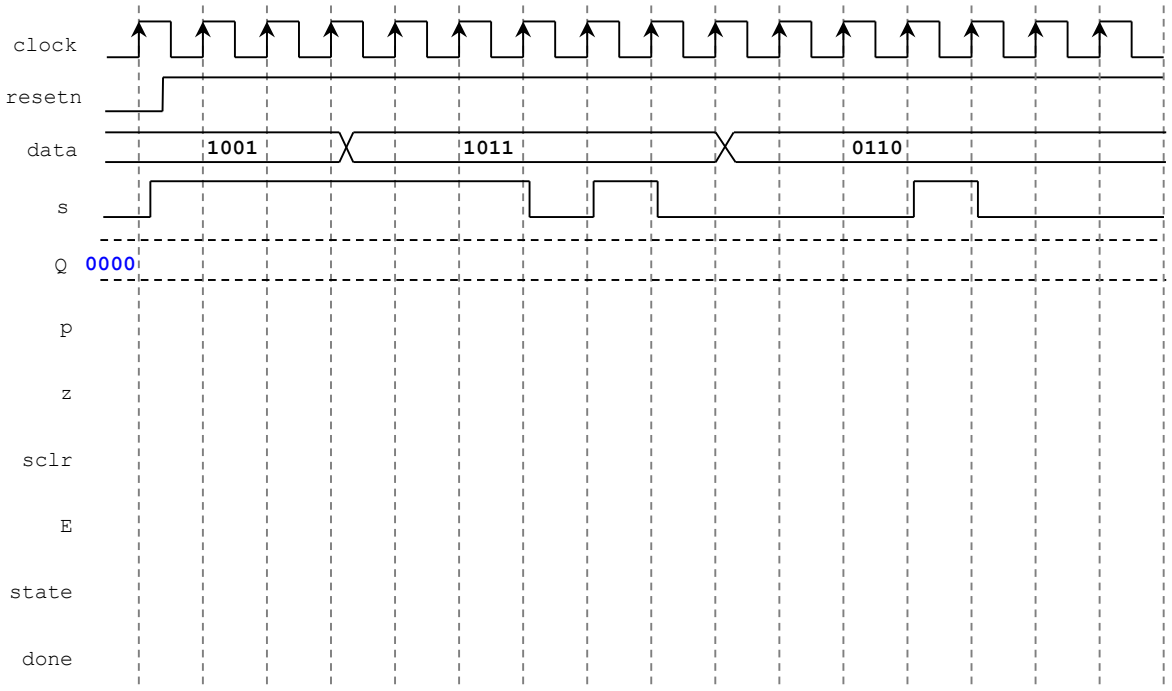
```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if a = '1' then
              if b = '0' then y <= S3; else y <= S1; end if;
            else
              y <= S2;
            end if;

          when S2 =>
            if b = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if a = '1' then y <= S2; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if a = '1' then z <= '1'; end if;
         when S2 => w <= '1';
         when S3 => if a = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```



PROBLEM 4 (20 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.





PROBLEM 5 (15 PTS)

- Attach a printout of your Project Status Report (no more than three pages, single-spaced, 2 columns). This report should contain the current status of the project. You **MUST** use the provided template (`Final Project – Report Template.docx`).